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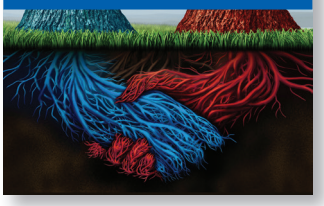


An innovative plating system

for next generation packaging technologies

MultiPlate:

An innovative solution for next generation packaging technologies

As device geometries continue to shrink, semiconductor packaging technologies face constant challenges to remain relevant and economically viable. Need of the hour is to develop innovative approaches that cost-effectively address the emerging requirements.

PRESSURE on the entire supply chain is rising and the drivers are clear – enhanced performance, more functionality, and reduced costs. Investments in next generation node technologies are perhaps too substantial and precarious and thus, the industry is turning to advanced packaging to enable improved performance and functionality.

While it is still unclear which of the advanced packaging technologies offer the best performance at the lowest cost, it is imperative that companies actively engage and peruse the multiplicity of options, as opportunity costs are significant.

Therefore, the industry and companies are evaluating a range of technical solutions to meet the current demands for advanced packaging. Accordingly there are many R&D assessments being undertaken using a variety of applications: fan out/in wafer level packaging (FOWLP, FIWLP), flip chip, fan out panel level packaging (FOPLP), embedding dies, 2.5D interposer, wafer level chip sized package (WLCSP), among many others. The challenge for packaging researchers and manufacturers is to develop technologies that are leading edge, relevant for contemporaneous market trends, and profitable, all while minimizing opportunity costs.

There is certainly one thing on which all agree – there is a dire need to develop new solutions to meet the future challenges for advanced packaging. This article will explore some of the those challenges and how they can be overcame by rethinking traditional manufacturing approaches.

High speed copper pillar plating for flip chip

As the “More than Moore” approach gains momentum, advanced packaging applications are more heavily scrutinized. Once a mainstay, traditional wire bonding is being surpassed by flip chip as the preferred packaging application for sub 45nm node technologies. Since its introduction flip chip has gained considerable market share and has proven to be technically superior to traditional wire bonding which requires a larger footprint and offers limited

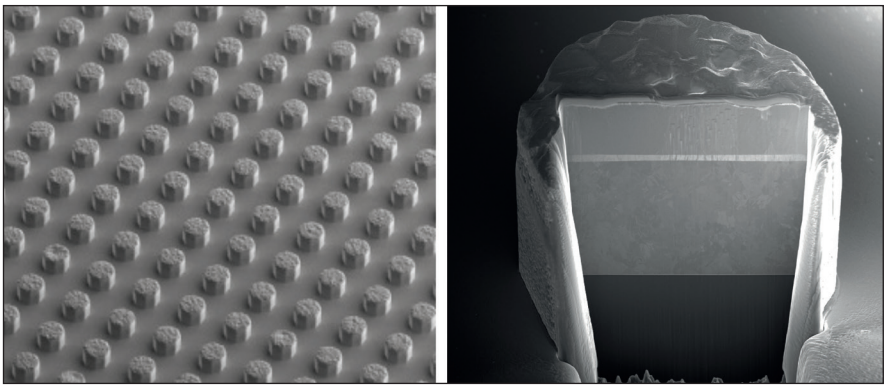


Figure 1: Example of Cu pillars with Ni barrier and Sn solder layers: (left) Top down view; (right) FIB SEM

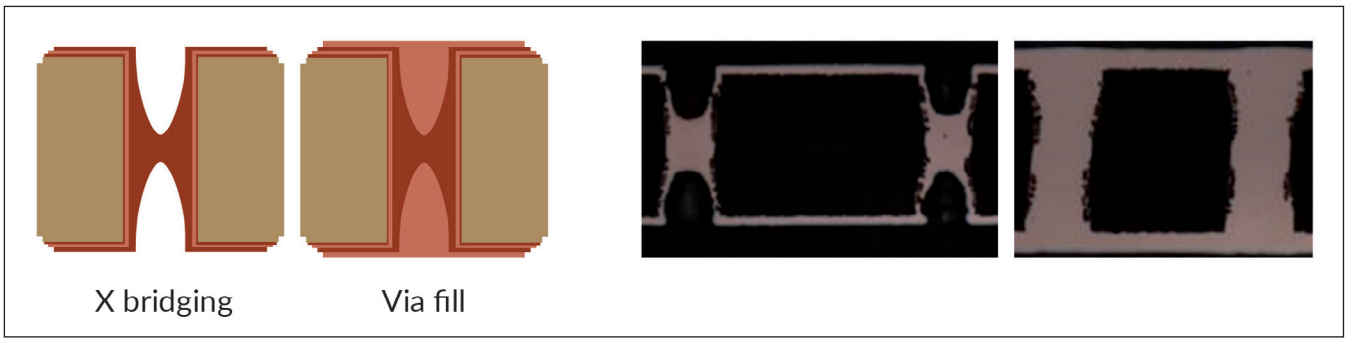


Figure 2: Atotech's patented "X bridge" through hole filling process; (left) graphic representation; (right) FIB cut of 200x100 μm through holes in panel size organic substrate

I/O density. More importantly, thermal and electrical performances are significantly improved with flip chip. Already in high volume manufacturing, flip chip currently represents roughly 16 percent of the overall packaging market (200mm equivalent). The projected flip chip growth is sizeable, with a steady increase in wafer starts over the next five years.

There are several ways to connect the flip chip to the substrate prior to packaging. The primary two methods are soldering and using Cu pillars. Soldering is utilized in flip chip BGA which uses SnAg balls to connect the chip to the substrate. The different soldering methods have a few limitations – C4 side paste printing is limited by solder paste and printing equipment, while micro ball placement has proven to be both slow and expensive.

For the most advanced technology nodes, the preferred interconnection technology in flip chip is Cu pillar. Market estimates suggest that in the coming years, Cu pillar technology has great potential and will lead the flip chip market segment in terms of growth. Two layers of Cu pillars connect the die to the IC package – a large pillar layer on the substrate side and a small pillar on the die side, followed by an optional RDL layer to further improve the I/O count. During plating, the Cu is electrochemically deposited to form the pillar according to the process requirements for height, diameter, and shape. Typically a thin electrolytic Ni layer (up to 3μm) is deposited on top of the Cu for the purpose of inhibiting diffusion and electromigration. Finally, the pillar is capped with electrolytic Sn or SnAg.

The standard process requirements for pillar plating include exceptional void performance, nonuniformity of less than 5 percent, and high current density plating at 10+ ampere per square decimeter (ASD). Each of these parameters contributes to the overall throughput, reliability performance, and yield for the plating process. Therefore, it is essential to develop a pillar plating technology that can deposit pure Cu with high deposition speed, without impacting the voiding performance and uniformity, both of which influence the electrical performance.

Atotech's unique MultiPlate in combination with their Spherolyte process satisfies all of the performance requirements for Cu pillar applications and provides a higher throughput than standard process of record, with a system throughput capacity of 50 wafers per hour. Using reverse pulse plating, the process is optimized to the desired pillar profile and shape, thereby reducing doming or dishing, and improving the overall uniformity of the deposited Cu (< 5 percent WIP/WID/WIW). In MultiPlate, deposition is significantly faster (≥20 ASD) than traditional fountain platers (≤10 ASD) and voiding performance is enhanced. Pure Cu depositions are made by possible by use of high purity chemistries and close monitoring of the bath components during plating. All of this is achievable because of the technically superior design of the system.

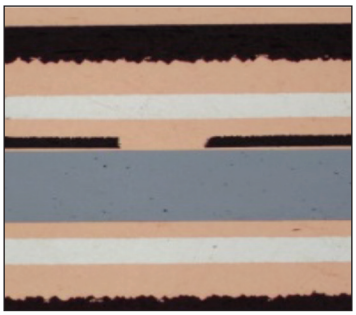
Cu through hole filling for interposer technologies

Although not currently used in standard wafer manufacturing, through hole filling (THF) is seen as a promising alternative for interposer manufacturing with large through silicon vias (TSV) as used in MEMS and image sensor applications. MultiPlate's THF technology allows for direct plating through substrates using the patented "X bridge" filling process, during which the deposited Cu forms an "X" at the center of the through hole, subsequently creating two vias that are then simultaneous filled using double side plating. This through hole filling process has been proven on glass, and Atotech also offers feasibility on wafer upon request. The primary advantage of the through hole filling process is the reduction of up to 30 percent of the process steps.

Double side plating for embedding components

For assembly technologies, embedding dies has been identified as a good solution for enhancing performance and reducing manufacturing costs. Embedding dies refers to the integration of components (passive components and integrated circuits) within the layers of a die package. Market research on embedded active and passive dies demonstrates that this technology will witness wide acceptance in the coming years, particularly for mobile

applications. Substrates with embedded dies offer smallest form factor and footprint, as the die package is significantly denser and therefore takes up less space on the PCB or IC substrate. Moreover, the process sequence, and in particular the number of plating steps, is shortened when dies are embedded and electroplated on both sides.



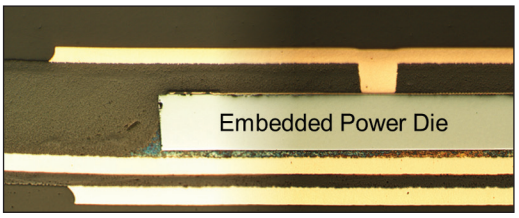


Figure 3: (left, right) Double side plated embedded power die; source: Fraunhofer IZM in collaboration with EmPower program

There are a number of other benefits of embedding dies, including higher levels of integration and improved thermal and electrical performance. Embedding dies facilitates a shorter electrical path, which results in a faster signal and overall electrical performance for the entire package. Embedding dies also presents the opportunity for increased levels of integration and the ability to house multiple dies, of various functionalities, in a single package.

Typically, during the embedding process, RDLs and backside metallization are done by sputtering and plating each side of the wafer or panel individually. This is a costly and equipment intensive exercise that can also slow down the production flow. MultiPlate's double side plating capability enables simultaneously plating of vastly different structures on each wafer or panel side, such as large pads for the back side metallization and fine lines of the RDL structures. This double side plating technique is successfully proven and well recognized for embedding power dies as part of the EmPower program.

Advanced Cu deposition will continue to be a mainstay in advanced packaging, but not without some limitations. A primary concern regarding Cu deposition is the fact that as the substrate thickness decreases and thicker Cu RDL layers are required (in FOWLP, for example), warpage is a critical processing challenge. Double side plating is able to overcome the warpage which is typical in high end processing with stress compensation achieved by simultaneous Cu depositions. The advantage here is significant, as warpage has a major impact on yield. Yield is also a challenge for panel-based manufacturing of embedded components. Notwithstanding, high volume manufacturers have already adopted embedded technologies for low I/O dies on panel-level. This will be discussed further in the next section.

RDL plating for fan out wafer/ panel level packaging

One example of embedding dies is fan out wafer/panel level packaging in which the die is placed on a wafer carrier and the package is built up around it. Fan out has been around for years and is a leading prospective trend for packaging manufacturing. More players are expected to increase capacity in the coming years for both ≥300mm

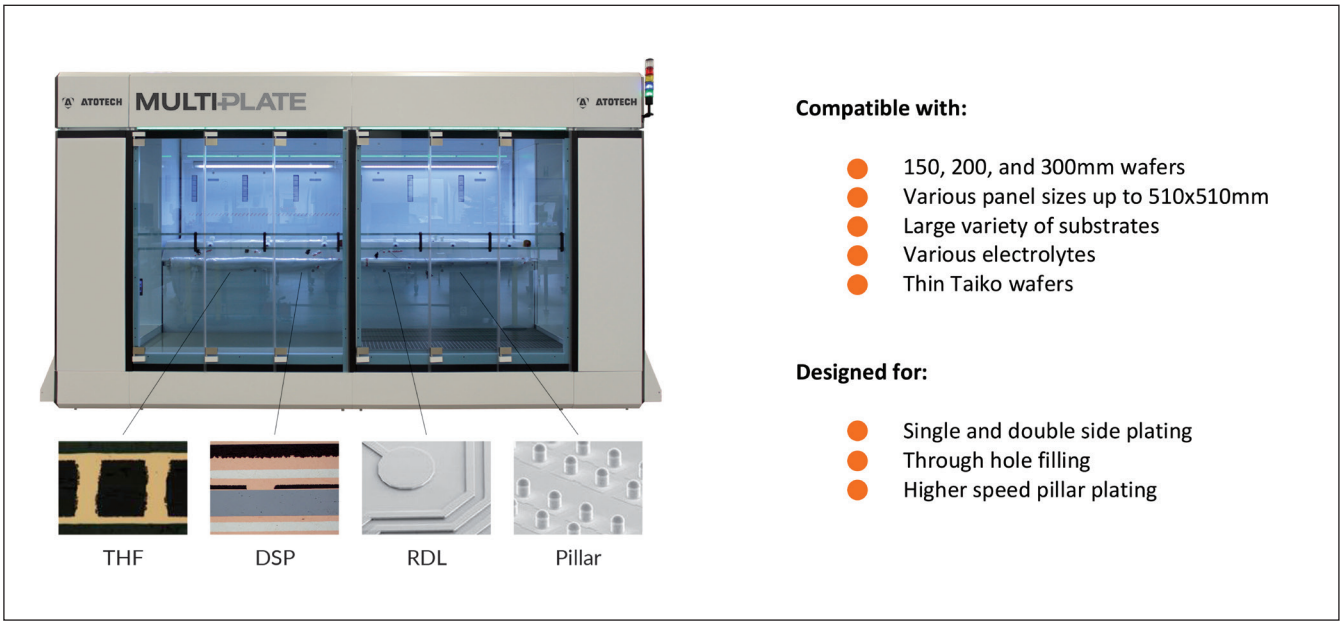


Figure 4: Tool process capabilities of the manual system offered by Atotech's MultiPlate. THF: Through Hole Filling, *DSP: Double Side Plating, RDL: Redistribution Layer, and Pillar

*Double side plating refers to the simultaneous plating of both substrate sides

wafer and panel applications. Fan out is a preferred packaging approach as it is designed to considerably increase I/O density with a reduced footprint and profile, partly due to the fact that it's thinner than flip chip, as it does not require a package substrate. In fan out processing, the redistribution layers are plated partially on the die and the molding resin. Using a metal or glass wafer carrier which is removed after plating, the RDLs and second layer interconnect (SLI) pads are left open to connect with solder balls to the PCB.

Warpage is a critical processing challenge in fan out due to the use of molding resins, thinner substrates, and thicker Cu depositions. Yet another challenge is posed by the lack of infrastructure. Both the equipment and complete fabs are unable to handle the large wafer and panel sizes, while continuing to provide desired yield.

Fan out processing may soon be done on panel level, as the price per piece significantly decreases from larger wafer sizes to panel. However, standard panel tools are not designed for processing wafers and tend to have a significantly lower yield than their wafer counterparts. This is partly due to the design of panel tools and the fact that they have not been engineered to satisfy the highest ISO standards.

MultiPlate is designed to satisfy the stringent requirements for next generation advanced packaging applications, both on wafer and panel level, and can also be customized according to the customers' production requirements. With its double side plating capability, it also effectively addresses the warpage issues.

MultiPlate: designed for performance

As manufacturing costs and yield become progressively critical for all members of the supply chain, performance of each process is of utmost importance. For high end ECD processes in packaging applications, yield, throughput, and reliability performance are optimized when the process, chemistry, on-line analytics, and plating equipment are in synchronization.

The primary requirements for high end, next generation ECD processes in packaging applications, as previously noted, include high purity deposits, nonuniformity of less than 5 percent, good voiding performance, and higher current density plating compared to what is currently available in the market.

The main processing challenges already discussed – the migration from wafer to panel, the issue of warpage when processing thin substrates, time sensitive production, yield, and most importantly – being able to quickly adapt for next generation technologies – can be overcome with MultiPlate.

MultiPlate is a next generation plating tool which offers the versatility and multi-functionality necessary to address the current and future challenges for optimal performance in advanced packaging technologies. It is an innovative electrochemical deposition plating system designed for flexible R&D and superior performance of high end application-specific production, and can be customized for through hole filling and both single and double side plating on RDLs and pillar structures which are required processes for many packaging applications such as flip chip, embedded power components including fan out, among many others.

MultiPlate's superior design includes the following features:

- **Dimensionally stable inert anodes for Cu plating:** An optimized uniformity within wafer/panel is enabled by an adjustable current distribution over the entire surface. This is possible due to the implementation of a segmented inert anode - two segments for 150 or 200mm and three segments for 300mm or panel.

- **Advanced fluid system:** Optimum electrolyte flow distribution is achieved with the advanced fluid system (AFS). The short distance from the cathode (wafer/panel) to the segmented anode provides a direct flow and superior agitation. Both of these are needed for high speed plating (current densities ≥20 ASD) and superior thickness uniformity.

- **Cu dissolving unit:** Voiding performance and uniformity are optimized by maintaining a bath with minimal impurity incorporation. By monitoring and replenishing the Cu concentration with an external unit while plating, there is no need to interrupt the production. Using intelligent software, algorithms, limits and frequencies of the measurements are specified in order to maintain an optimal plating result.

- **Free programmable mechanical agitation:** Overall uniformity is improved with the use of a freely programmable mechanical agitation mechanism. This mechanism allows for the movement of the wafer holder – down to just 35mm from anode to cathode – which eliminates the risk of spray and flow pattern, thereby improving uniformity.

Figure 5: Images of a manual MultiPlate system; (left) front view; (middle) plating baths; (right) chemical distribution units

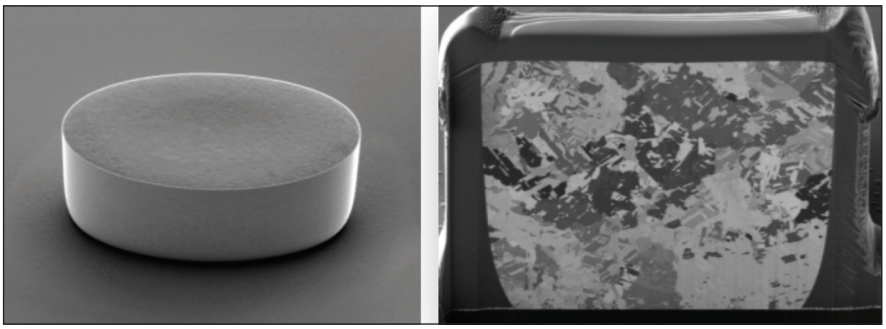


Figure 6: (left) Example of a 20 μm Cu pillar plated at 3.8 μm per minute; (right) FIB cut through the pillar

- **Multipurpose rectifier:** Reverse pulse plating is essential for high speed pillar plating to achieve an ideal profile (no doming or dishing), and to obtain Atotech's patented "X bridge" technology in through hole filling. The "X bridge" is achieved by double side plating the wafer/panel to form two blind vias on each wafer/panel side. Next the vias are filled using a standard electrolytic plating process. For double side plating processes, the current parameters can be independently adjusted for each wafer or panel side to support different design layouts and plated thickness requirements.

- **Substrate holder:** For dry contacting of 150, 200, or 300mm wafers and panels, substrate holders for both single and double side plating are available and are capable of handling thin Taiko wafers as well as glass.

- **Fast wafer handling:** The automated load/unload station is designed for high throughput – approximately 50 wafers per hour – with the final rinse and dry station after unloading.

- **Easy maintenance:** MultiPlate was designed for ease of use, employing intuitive human interface, and complying with the latest ISO and clean room standards. A completely encapsulated line and modular approach means that maintenance is streamlined with quick access to subunits.

Designed to deliver exceptional results

MultiPlate effectively complements Atotech's proven Spherolyte process to deliver unmatched ECD processes which enable an improved, cost effective manufacturing flow and better performance.

High speed copper pillar plating

- High speed pillar plating (≥20 ASD or 4 μm/min)
- Excellent uniformity (<5 percent WIW, WID, WIP)
- High purity Cu deposit
- Homogeneous Cu grain structure
- Superior voiding performance eliminates the need for Ni diffusion barrier on Cu pillar

Through hole filling capability

- Reduced process steps (≥30 percent) which means higher throughput
- Pulse reverse option allows filling of through holes

Double side plating for next generation assembly technologies

- Warpage compensation by simultaneously plating on both wafer or panel sides
- Reduced process steps (≥30 percent), eliminating manufacturing complexity
- Excellent uniformity (≤10 percent WIW)
- High purity Cu deposit
- Homogenous Cu grain structure

Planned market entry

Currently installed at the Berlin Technical Center, Atotech's MultiPlate system is fully operational and ready for additional wafer scale feasibility studies and POR determination on 150, 200, and 300mm wafers. The first automatic wafer system will be shipped in April 2016, while the first semi-automatic panel system will be delivered in July 2016.

Next generation packaging technologies

With the addition of MultiPlate, Atotech now holds the unique position of offering customers a one-stop-shop when it comes to electroplating, providing high purity chemistry, plating equipment, and process development for ECD packaging

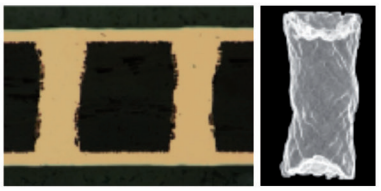
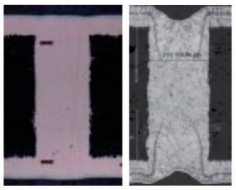
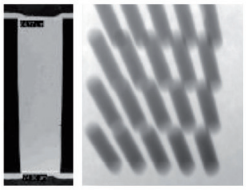
Substrate and Dimensions	Process Results
Organic substrate Panel 200 µm by 100 µm through holes 2 : 1 aspect ratio (AR) 60 min process time	
Organic substrate 200 mm wafer 275 µm by 115 µm through holes 2.4 : 1 AR 80 min process time	
Glass substrate 200 mm wafer 290 µm by 80 µm through holes 3.6 : 1 AR 95 min process time	

Figure 7: Various images of through hole filling with corresponding filling times, dimensions, and aspect ratios

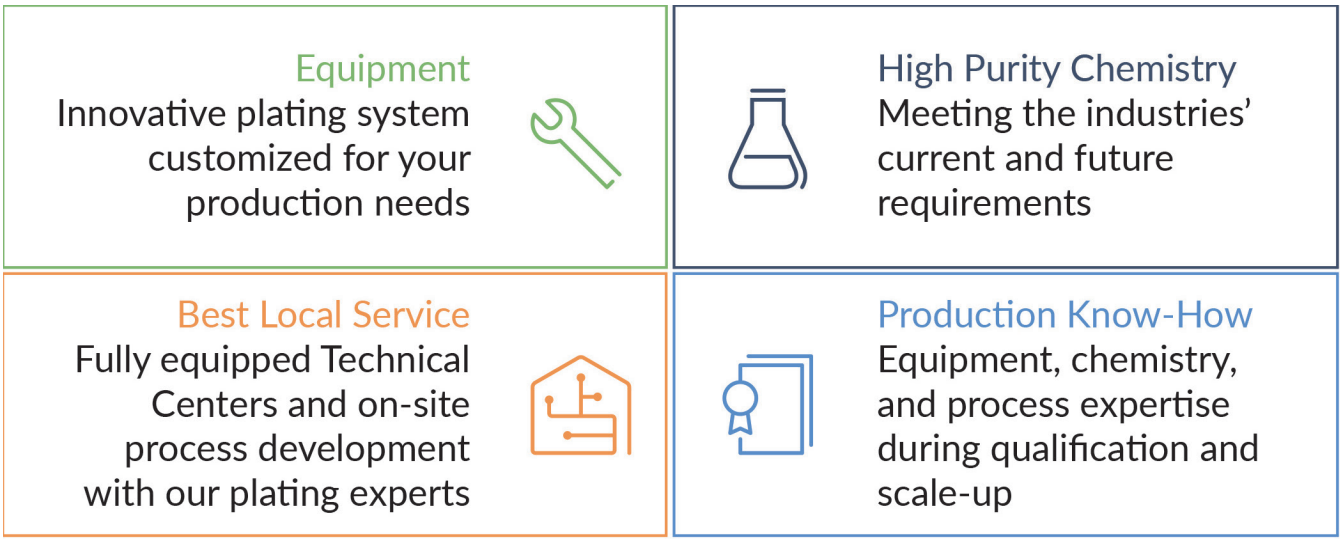


Figure 8: The four pillars of Atotech's semiconductor business strategy

applications. The company's journey began with the transfer of know-how from their industry leading plating processes and equipment for single and double side plating on printed circuit boards, to the optimization of these technologies for semiconductor packaging applications at their Berlin Technical Center.

Atotech has provided the electronics industry with leading technology solutions – including highly specialized chemistries and plating equipment – for over a century. Their in depth plating know-how is built on a comprehensive legacy of M&T Chemicals and Schering Galvonotechnik. Over the years, Atotech has remained committed to developing technologies which are measurably superior, ecological, and competitively priced. Staying ahead of the competition and being able to address the industry's demands for next generation technologies has always been the foundation of Atotech's global strategy. Thus, the migration to the semiconductor equipment market was only a natural and essential undertaking. Atotech's semiconductor capabilities have steadily grown since its inception in 2006. The success of its semiconductor division is reflected in their consistently expanding global network and client base.

The company's strength lies not only in their comprehensive know-how and leading technology solutions, but also in their highly trained team of experts and an ability to stay close to the customer.

Their Technical Center and Systems approach – with regional Technical Centers equipped with plating manufacturing equipment and managed by technology experts – enables them to support customers at all key locations globally.

Their decision to expand focus to include advanced packaging equipment was made primarily with the intent to offer customers a one-stop-shop, and to explore unchartered territories in semiconductor manufacturing: double side plating on wafer and panel, plating on glass and organic substrates, and high speed pillar plating using the well-known reverse pulse system.

With MultiPlate, Atotech has yet again raised the bar in providing pioneering solutions to tackle key challenges facing the industry today. It is decidedly superior to conventional plating tools available for standard RDL or pillar plating on the market, and offers key features and capabilities for overcoming the obstacles that next generation technologies will present.

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> "Over the years, Atotech has remained committed to developing technologies which are measurably superior, ecological, and competitively priced. Staying ahead of the competition and being able to address the industry's demands for next generation technologies has always been the foundation of Atotech's global strategy"