Stannatech® IC

Immersion tin for IC substrates

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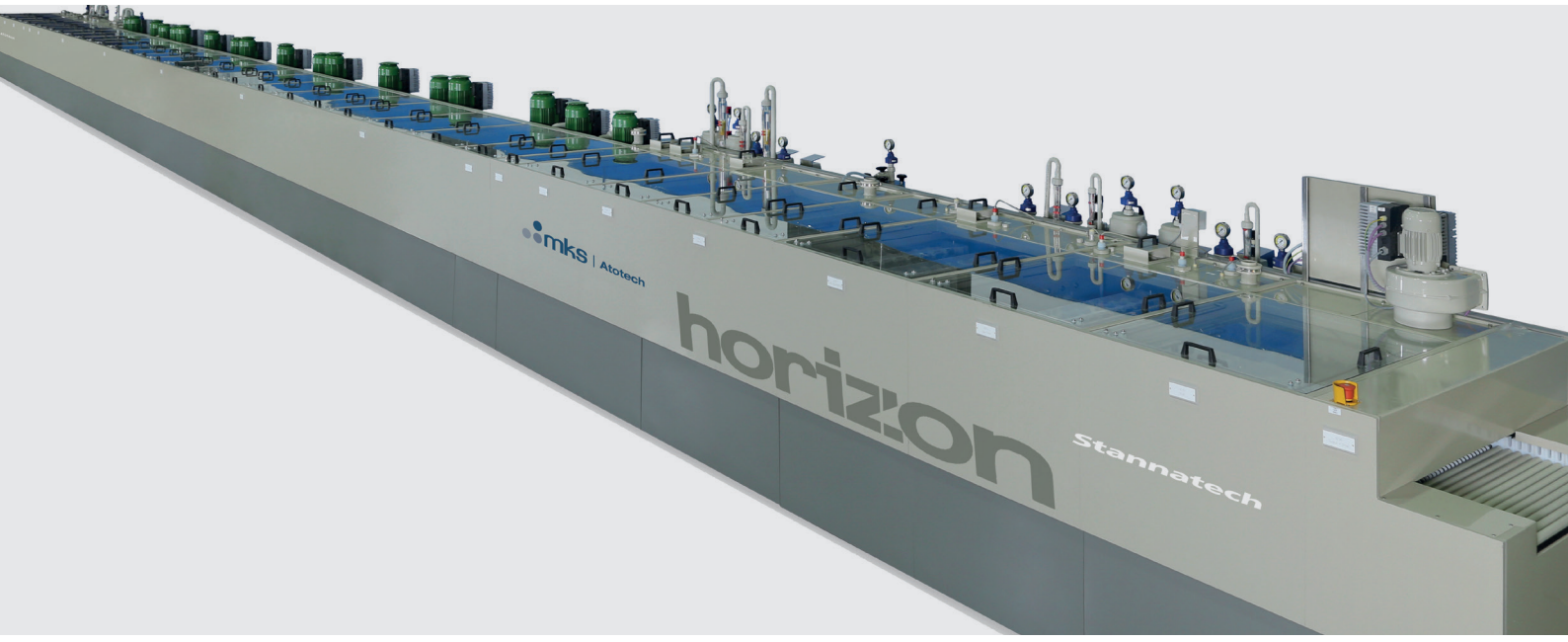

The next generation of Stannatech®

Immersion tin for package substrates

Stannatech® IC aims to further optimize the existing Stannatech® immersion tin chemistry for package substrate specific i-Sn baths. Due to the reduced viscosity, the process reduces the soldermask attack and the copper dissolution. Stannatech® IC has superior performance to 2000V in regard to foaming and is therefore easy to control.

Benefits at a glance

- Optimized metal ion exchange
- Missing bump reduction
- Ultimately controllable
- Rinse contamination by chemistry and drag out is optimized

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Figure 1-3:
Maximized filling potential
Minimized copper dissolution
IC bump capable

Maximized filling potential

Higher metal content in the solution induces the filling of microstructures under low exchange conditions. The plating takes place preferentially before the solder masks/copper attack. Thanks to reduced solution viscosity the solution exchange is optimized. This helps to prevent cavities and maximizes filling potential.
At the same time, lower viscosity leads to reduced rinse contamination and drag out. It thereby ensures controlled horizontal processing with fine feature designs.

Market leading process control

Stannatech® IC is designed to work with market leading auxiliary equipment like Crystallizer® and Constannic®. This allows a controlled deposition speed by the continuous removal of copper. It also reduces the risk of rinsing problems or issues caused by Cu redeposition. With the implementation of the Constannic® system, sludge can be reduced and the risk of equipment problems caused by e.g. blockages can be minimized.

IC substrate specific benefits

- Fine L/S capability
- No missing bumps
- Low viscosity
- Low solder mask attack
- Low copper dissolution